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High Performance Low Latency Parallel Successive Cancelation Decoder Structures for Polar Codes

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Keywords	Abstract
Multi-Parallel SCD Polar Coding BEC	Polar codes are decoded using successive cancellation (SC) algorithm where likelihood ratios (LRs) for data bits are calculated in a sequential manner, and decisions are made using the calculated LRs. During the decoding of an information bit, the decision results for the predecessor bits are used, and a wrongly decided predecessor bit has negative effect on the accurate calculation of the LR for the information bit being decoded. In SC algorithm, when LR=1, the information bit is decoded as uˆ_i=0, however, such a decision has 50% of chance of being correct. In this paper, we propose improved polar decoders utilizing a number of SC decoders. We consider the case of LR=1, and propose polar decoder structures for the more accurate calculation of the LRs of the successor bits.

1. Introduction

Polar codes invented by Arikan [1] is the primary class of error correcting codes that can provably achieve the capacity of binary discrete memoryless channel (B-DMC) when the code length approaches to infinity. Polar codes are decoded in a recursive manner using successive cancelation list (SC) algorithm. The successive cancellation list (SCL) introduced in [2] shows significant performance improvement compared to SC decoding. In an SCL decoder, both 0 and 1 are considered as estimated bits and two decoding paths are generated at each decoding stage. The cyclic redundancy check (CRC) is used in [3, 4] to select the correct decoding path in the SCL algorithm. However, SCL decoding has much higher decoding complexity [5, 6] compared to SC. In this paper, we propose new decoding approach for polar codes considering the case of LR=1. The proposed method employs multi-SC decoders constructed in parallel with enhanced decision functions to correct the lost bits that in turn leads to an increase in error propagation. The proposed technique provides a flexible configuration, and leads to pruning of unnecessary path searching operations, which reduce the decoding complexity. Multi-Parallel SC decoding show a significant performance improvement compared with the original SC decoding.

2. Preliminaries and Notations

Binary discrete memoryless channels (B-DMC) is considered for illustrative purposes in this paper. In this paper we write $W: X \to Y$ to denote a generic binary discrete memoryless channel (B-DMC) with input alphabet X, output alphabet Y and transition probabilities $W(y|x)$, $x \in X$, $y \in Y$. For a BEC, the input alphabet X is chosen from the binary set $\{0, 1\}$ while Y and the transition probabilities may take arbitrary values. In the paper, $y_1^N = (y_1, y_2, ..., y_N)$ are the observations of the code bits $x_1^N = (x_1, x_2, ..., x_N)$, obtained via encoding of the information bits $u_1^N = (u_1, u_2, ..., u_N)$, through N copies of the channel W.

3. Successive Cancellation Decoding

At the destination side, using the received word $y_1^N = (y_1, y_2, \ldots, y_N)$, information bits are estimated successively using the likelihood ratios (LRs) of the bits appearing in code structure. In this paper, binary erasure channel is employed for performance evaluation. A bit transmitted through binary erasure channel is either received correctly with probability $1 - \epsilon$ or lost with probability ϵ. It is shown in [1] that the LRs of the information bits can be recursively as.

$$L_N^{(2i-1)}\left(y_1^N, \hat{u}_1^{2i-2}\right) = \frac{L_{\frac{N}{2}}^{(i)}\left(y_1^{\frac{N}{2}}, \hat{u}_{1,o}^{2i-2} \oplus \hat{u}_{1,e}^{2i-2}\right) L_{\frac{N}{2}}^{(i)}\left(y_{\frac{N}{2}+1}^N, \hat{u}_{1,e}^{2i-2}\right) + 1}{L_{\frac{N}{2}}^{(i)}\left(y_1^{\frac{N}{2}}, \hat{u}_{1,o}^{2i-2} \oplus \hat{u}_{1,e}^{2i-2}\right) + L_{\frac{N}{2}}^{(i)}\left(y_{\frac{N}{2}+1}^N, \hat{u}_{1,e}^{2i-2}\right)} \tag{1}$$

$$L_N^{(2i)}\left(y_1^N, \hat{u}_1^{2i-1}\right) = \left[L_{\frac{N}{2}}^{(i)}\left(y_1^{\frac{N}{2}}, \hat{u}_{1,o}^{2i-2} \oplus \hat{u}_{1,e}^{2i-2}\right)\right]^{1-\hat{u}_{2i-1}}$$
$$\times L_{\frac{N}{2}}^{(i)}\left(y_{\frac{N}{2}+1}^N, \hat{u}_{1,e}^{2i-2}\right) \tag{2}$$

The decision is made according to

$$\hat{u}_i = \begin{cases} 0 \; if \; LR(\hat{u}_i) \geq 1 \\ 1 \; otherwise \end{cases} \tag{3}$$

Where $LR(\hat{u}_i)$ is defined as

$$LR(\hat{u}_i) = \frac{Prob(\hat{u}_i = 0|y)}{Prob(\hat{u}_i = 1|y)}$$

4. Proposed M-Parallel SC Decoding Algorithm

In SC decoding of polar codes [1], whenever $LR(\hat{u}_i) = 1$ the decision is made as $\hat{u}_i = 0$ according to (4). However, in such an approach, we have 50% of making a correct decision. A wrong decision will certainly have negative effects on the determination of the successive bits. Considering this issue, we propose multipath parallel structures for SC decoding operations.

4.1. Multi-Parallel SCD (MP-SCD) for M=2

Successive cancelation decoding operation is a sequential decoding operation. The decoding decision for the ith bit, u_i, affects the decoding decisions of the successive bits, i.e., bits $u_j, j > i$. Absolute value of the log-likelihood ratio, i.e., $|LLR|$, is an indicator for the accuracy of the decision. Large $|LLR|$ implies a more robust decision. And a wrong estimation for the information bit u_i will push the values of $|LLRs|$ towards 0 for the successive bits.

To alleviate the information loss and improve the decision robustness, considering the case of $LR(u_i) = 1$, we propose a structure as depicted in Fig.1 where we utilize two SC decoders, one of which uses the decision logic.

$$PD_1: \hat{u}_i = \begin{cases} 0, \; if \; LR(u_i) = 1 \\ 0, \; if \; LR(u_i) > 1 \\ 1, \; otherwise \end{cases} \tag{4}$$

Whereas the other employs

$$PD_2: \hat{u}_i = \begin{cases} 1, & if \ LR(u_i) = 1 \\ 0, & if \ LR(u_i) > 1 \\ 1, & otherwise. \end{cases} \tag{5}$$

Once the decoding operation for all information bits is complete, sum of the absolute log-likelihood ratios, i.e.. LLRs, is performed according to

$$S_{PD_1} = D1: \sum_i |LLR_i| \quad S_{PD_2} = D2: \sum_i |LLR_i| \tag{6}$$

Where LLR_i indicates the log-likelihood ratio for information bit u_i for the corresponding decoders. The winner decoder is chosen considering

$$PD_w = \begin{cases} PD_1 & if \ S_{PD1} \geq S_{PD2} \\ PD_2 & otherwise. \end{cases} \tag{7}$$

The estimated bits of the winner decoder are accepted as the result of the decoding operation. The overall logic for the proposed decoding operation is illustrated graphically in Figure.1 and Figure.2.
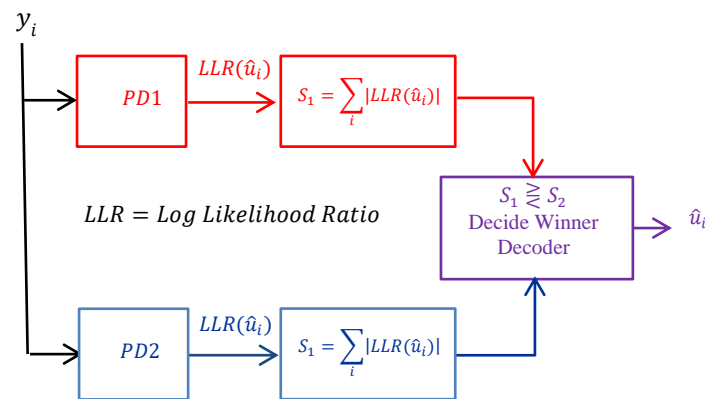
Figure 1. Block Diagram For M=2 Parallel Sc Decoding Operation

The structure shown in Figure.1 corresponds to the case $M = 2$ i.e., we have two parallel decoder. The sum of the absolute values of the LLRs is calculated for each decoder, and the decoder with larger summation result is chosen for decision operation. Unlike to the SC decoder where only one path is reserved at each level, the multi-parallel algorithm utilizes M different searching paths. Therefore, it is more likely for the m-parallel algorithm to find the desired path than the SC algorithm. In Figure.1 (a) and Figure.1 (b), two examples for N = 8 considering $LR = 1$ cases are depicted.

   The example depicted in Figure.1 (a) illustrates the worst case. It is seen from the example that the decoded sequences can be 000 or 111, in this case just the first bit can be exactly correct and the number of paths is not greater than M=2. In the example depicted in Figure.1 (b), the 1st, 3rd bits are lost and the 2nd bit is normally detected as 1.

$$if\ (LR = 1)$$
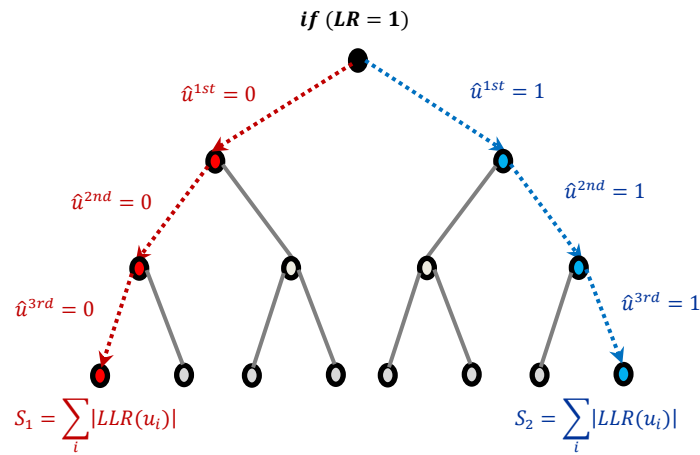
Figure 1. (A) Decoding procedure in Case 1, where the $1^{st}, 2^{nd}$ And 3rd bits are lost.

The possible decoded words can be {010,111}. In the decoded sequence, the first and second bits are true, but the third bit can be true with probability of 0.5.

In this case we note that the path searching is changed by the second bit for which it is assumed that $LR < 1$. The path having the highest absolute logarithmic likelihood sum is chosen for the determination of the decoded sequence.

$$if\ (LR = 1)$$
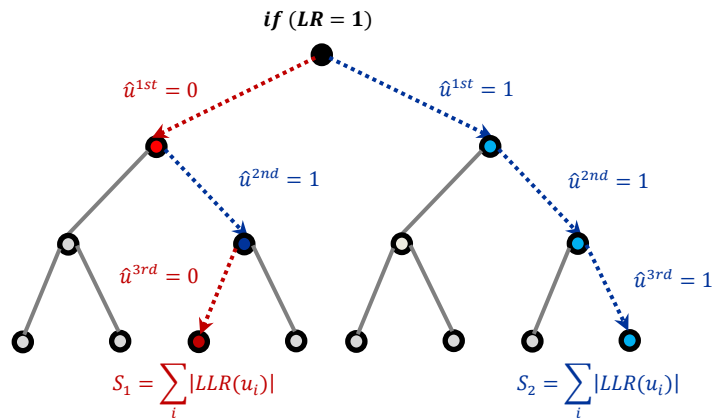
Figure 1. (B) Decoding procedure in Case 2, where the 1st and 3rd bits are lost but the 2nd bit is normally detected as 1.

4.2. Multi-Parallel SCD (MP-SCD) for M=4

To improve the decision accuracy, we can increase the number of parallel decoders which handle $LR(u_i) = 1$ case in different ways. In Figure.2, multi-parallel SCD structure for $M = 4$ is depicted.
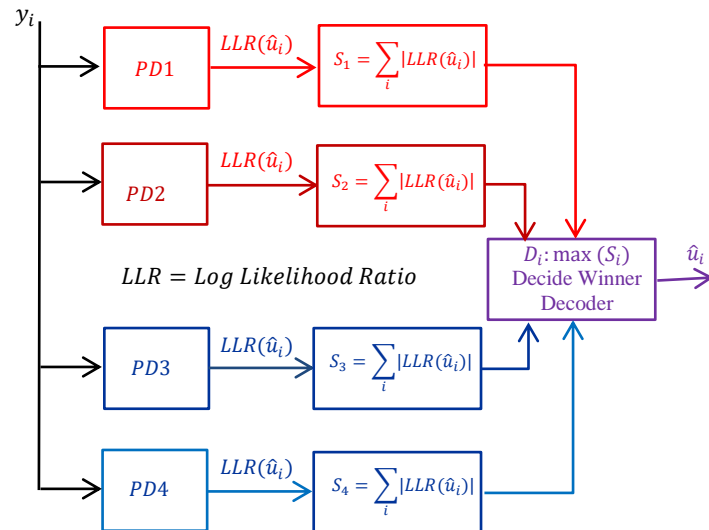
Figure 2. Block diagram for M=4 parallel Sc decoding operation.

In Figure.2, PD_1 always makes the decision '0' when LR=1, PD_2 makes the decision '0' only once when LR = 1, and it makes the decision '1' for the other LR=1 cases, PD_4 always makes the decision '1', PD_3 makes the decision '1' only once when LR = 1, and it makes the decision '0' for the other LR=1 cases. Two examples for M=4 are provided in Figures 2(a) and 2(b).
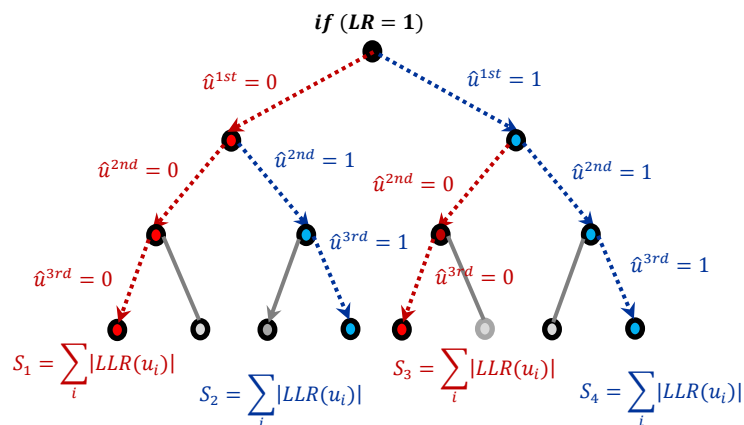
Figure 2. (A) Decoding procedure in Case 1, where the $1^{st}, 2^{nd}$ and 3rd bits are lost.

In Figure. 2(a) for M=4, we consider the case where the first 3 bits are erased, and in this case the candidate sequences for the decoder output are {000, 110, 001, 111}. For the example of Figure.2(b) for M=4, we consider the case where the 1st and 3rd bits are lost but the 2nd bit is normally decoded as 1, and in this case the candidate sequences for the decoder output are {010, 110, 011, 111}. As it is clearly seen from Figure.2(b) search path is altered by the second bit which acts as a path corrector, and the winner path has the largest absolute logarithmic likelihood sum.
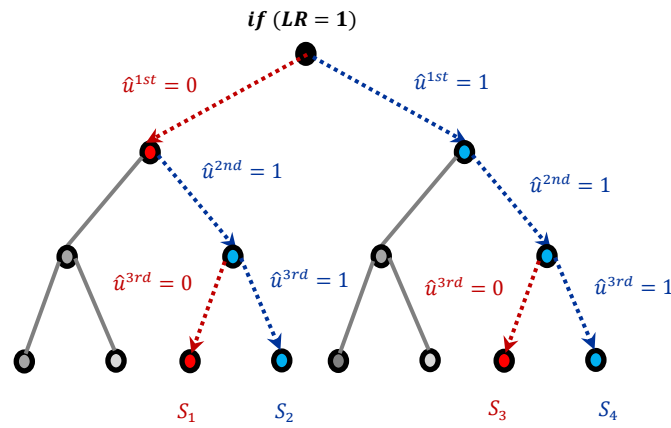
Figure 2. (B) Decoding procedure in Case 2, where the 1st and 3rd bits are lost but the 2nd bit is normally detected as 1.

5. Simulation Results

Computer simulations are performed using frame length of 1024 and 128 for binary erasure channels having erasure probabilities 0.5, and bit-error-rate (BER) and frame-error-rate (FER) performance curves for moderate frame lengths are obtained as shown in Figures.3, 4 and Figures.5, 6 respectively. It is seen in Figure. 3 that, two types of simulation curves are available.

In figures, the lines with label '*' indicates the simulation results assuming that perfect channel knowledge is available at the receiver side, and if the sequence associating with one of the decoded paths matches the transmitted frame, it is accepted as the decoder result, otherwise, the path having the largest absolute LLR sum is chosen. It is seen from the performance curves that the code performance increases as the number of parallel branches increases, and when parallel branch number is 4, the performance of the proposed method approaches to the performance for which perfect channel knowledge is available. We obtain significant performance improvement over (SCD).
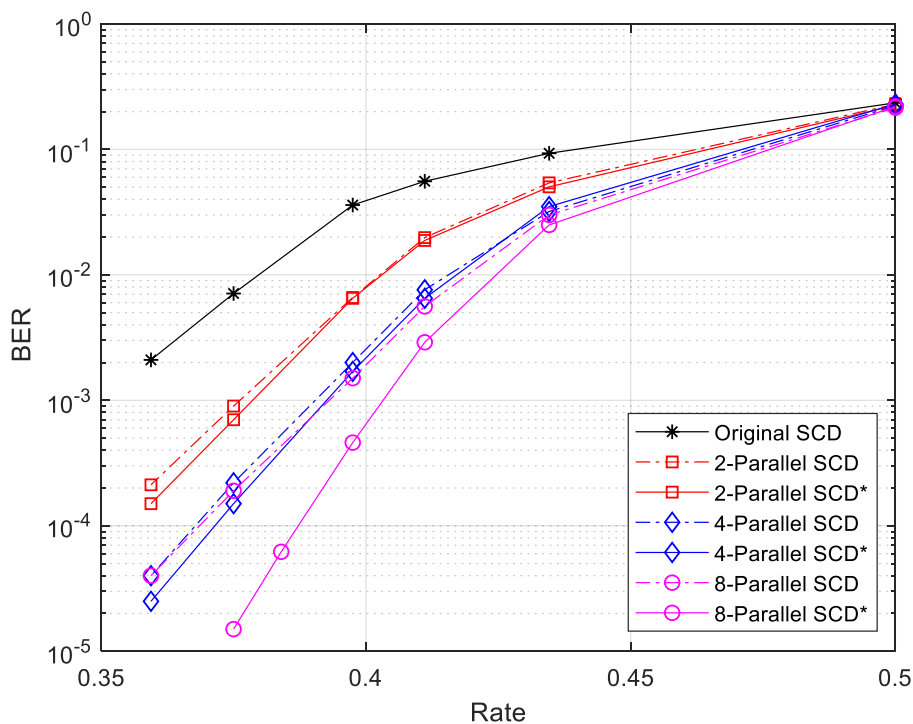
Figure 3. BER performance under different M size for frame- length P(1024) over binary erasure channel.
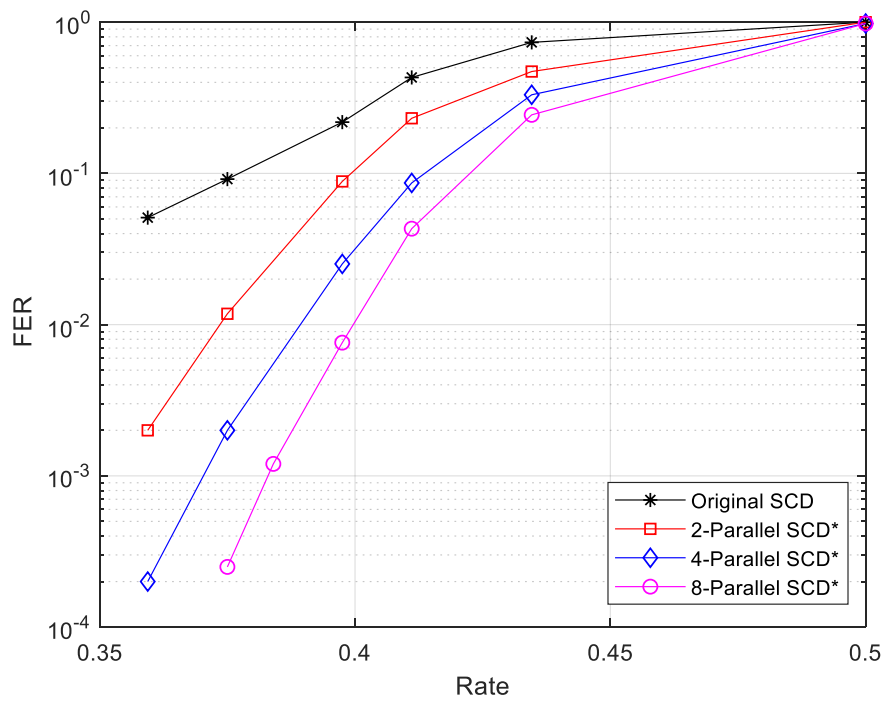
Figure 4. FER performance under different M size for frame- length P(1024) over binary erasure channel.
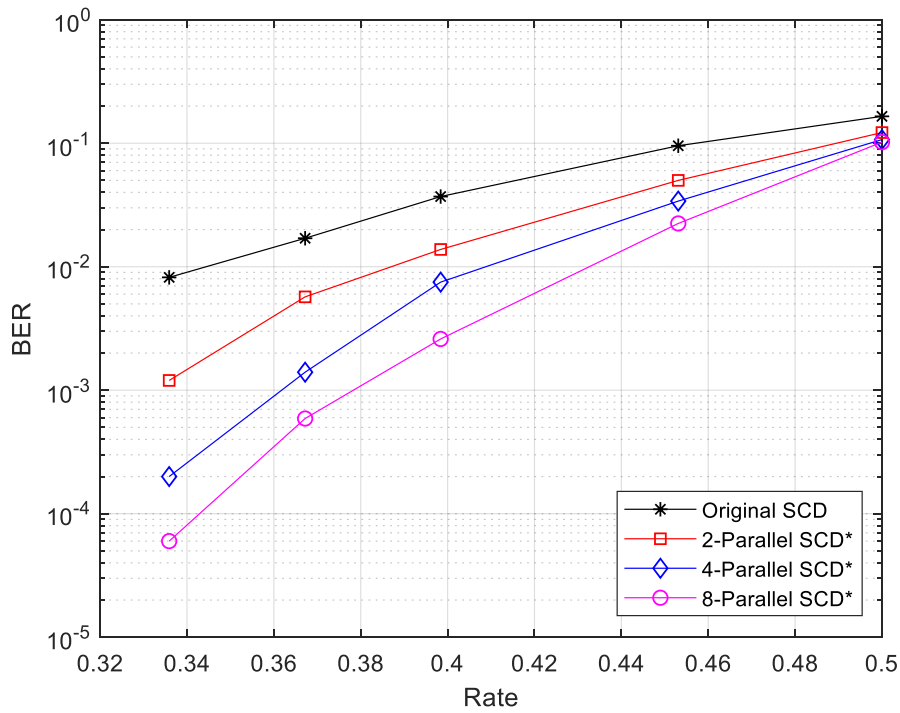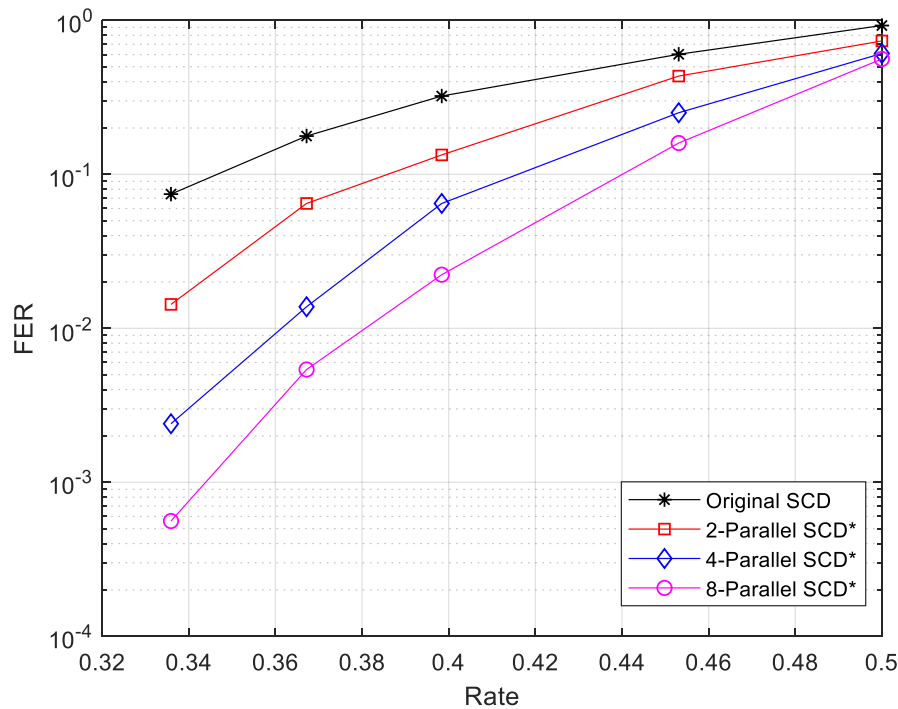

Figure 5. BER performance under different M size for frame- length P(128) over binary erasure channel.

Figure 6. FER performance under different M size for frame- length P(128) over binary erasure channel.

6. Conclusions

In SC decoding of polar codes, when LR=1 for an information bit, the decision is made in the favour of 0, however, in such a decision an uncertainty occurs, and in this instance polar decoder has 50% chance of making a correct decision. Considering this circumstance, we proposed novel polar decoding methods, which considers two decisions i.e., '0' and '1', for LR=1 at the node of the decoding tree.

In one approach, path doubling is only done once when LR=1, which corresponds to two parallel decoders, i.e., M=2. And, in the next approach, we considered path doubling twice, i.e., a path doubling is made when LR=1, and another path doubling is made when LR=1 and no more, which corresponds to four parallel decoders, i.e., M=4. Simulation results indicate that the proposed approaches show significant performance improvement over classical SC decoder

Declaration of Competing Interest

The author declares that there is no competing financial interests or personal relationships that influence the work in this paper.

Authorship Contribution Statement

Abdelkareim Abulgaasem A. ALRTAIMI: Conceptualization, Methodology, Software, Investigation, Resources, Writing - Original Draft.
Orhan Gazi: Validation, Formal analysis, Supervision.

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