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Design Consideration for Active–Only Memcapacitor Emulator Circuits

Hacer Atar Yildiz and Omer Aydin

Abstract—**In this paper, a simple memcapacitor emulator circuit using only active elements is presented. Instead of using any bulky passive components, the proposed circuit makes use of the intrinsic capacitors of MOSFETs. As a result, the circuit took up significantly less area on the IC environment. In addition, a modification technique is proposed to extend the operating frequency range of the emulator, which might broaden the circuit's application possibilities. Considering the basic non-idealities of the circuit, a more realistic formulation of the memcapacitance value is derived. Detailed simulations utilizing the 0.18 µm CMOS Cadence design tool are used to validate all theoretical aspects as well as the circuit's appropriate functionality.**

Index Terms—**Memcapacitor emulator circuit, pinched hysteresis loop, CCCII, electronically adjustable circuit**

I. INTRODUCTION

MEMRISTOR was first postulated by L. O. Chua as the missing circuit component in 1971 [1], is shown to be physically realizable by HP in 2008 [2]. Later, with the introduction of new class of mem-elements, memcapacitor and meminductor by Chua [3], the application of these elements has been expanded further for instance in adaptive filters [4], oscillators [5], chaotic circuits [6-7], neuromorphic circuits and non-volatile memories [8-10].

As the memristive elements are characterized by the well-known pinched, or zero-crossing hysteresis twist in current-voltage space, the fingerprint of the memcapacitor is the pinched loop in the voltage-charge space [11]. In some implementation, memcapacitor behavior can be obtained using mutator which converts memristor behavior to memcapacitor [12-13]. These circuits employ perfect memristor to implement the memcapacitor, which may be problematic in

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case the limitations of the involved memristor are not well understood or its optimized design is not available. The synthesis of memcapacitor using conventional building blocks, i.e. integrators, summing amplifiers, on the other hand, is a more prudent approach as the optimized basic building blocks are easily accessible [14-17].

At this point, it should be noted a well-known disadvantage of all these mem-element emulators for IC integration point of view, which stems from the implementation of the involved passive elements, suffer from large chip area [18-20]. Active-only circuit design is a very useful technique to address this drawback. In these circuits, passive components are realized using the intrinsic resistors and capacitors of the involved active components [21]. While this approach substantially reduce the chip area occupied by the circuits, the circuit parameters can be adjusted electronically.

In this study an area efficient implementation of an integrator-based memcapacitor emulator (MC) is introduced. In order to have an area efficient solution, a design containing only active components is proposed. The benefits of the circuit are revealed by comparing it with similar circuits presented in the literature. Thanks to the evaluations of the main non-idealities of the proposed circuit, theoretical considerations which may help to assess the limitations of the proposed circuit are presented. Simulation results of the circuit using UMC 0.18 µm CMOS process are presented to illustrate the circuit performance.

In this paper, first the proposed realization of the memcapacitor emulator is presented. Then, the active element nonidealities are modeled and theoretical expressions are derived, which may be useful to assess the circuit important limitations. The operating frequency range of the proposed emulator is considered to be limited, which is partially mitigated by applying a modification technique. Simulation results justifying the proper operation of both the initial and the modified circuits are presented. Finally, a section with extensive comparisons of the suggested circuits to their counterparts is provided.

II. PROPOSED MEMCAPACITOR EMULATOR AND ITS PRELIMINARY DESIGN CONSIDERATIONS

The proposed memcapacitor, consisting of two active integrators built around a second generation current conveyor (CCII), a current controlled current conveyor (CCCII) and two voltage buffers is given in Fig.1. Note that CCCII is actually a

modified CCII, in which the intrinsic x-terminal resistance is included in its defining equation.

This resistance is given by:

$$r_x = \left(\mu_n C_{ox} \frac{W}{L} I_B \right)^{-1/2} \tag{1}$$
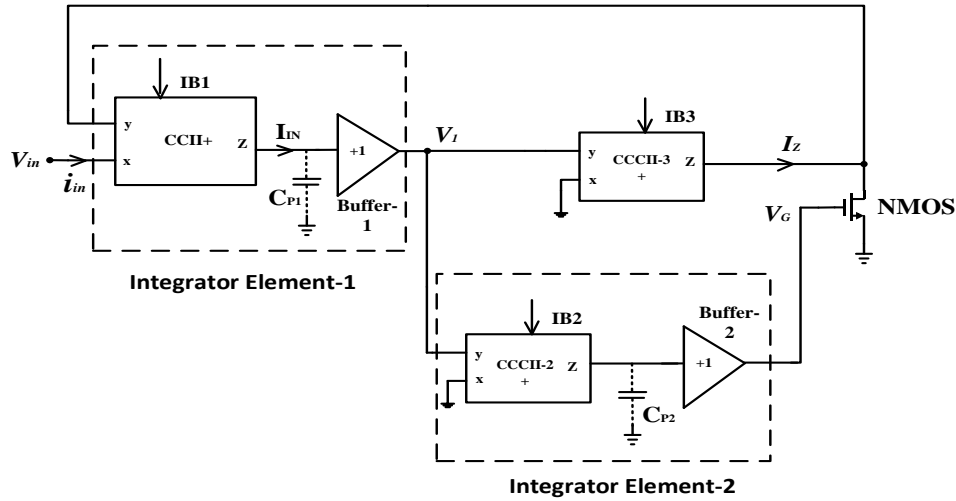

Fig.1. The general topology of proposed MC topology

From Fig. 1, capacitors, C_{P1} and C_{P2} shown within the dashed lines are intrinsic capacitors which appear at the input port of the voltage buffers. While designing the circuit, transistors' dimensions at the input section of the voltage buffer are chosen big enough that these intrinsic capacitors become large and dominate other parasitic capacitors in the circuit. Moreover, in case the voltage buffers are implemented such that properly, these capacitors mainly stem from the gate capacitance of MOS transistors, these capacitors can be considered linear [22]. Given the formal defining equations of CCCII and CCII, respectively [23],

$$\begin{bmatrix} I_y \\ V_x \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & r_x & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_Z \end{bmatrix}, \quad \begin{bmatrix} I_y \\ V_x \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_Z \end{bmatrix} \tag{2}$$

and considering the fact that the input voltage V_{in} is small enough to satisfy $(V_{DS} \ll V_{GS} - V_{TN})$, the equivalent memcapacitance value of the proposed MC can be obtained as follows:

$$V_1 = \frac{1}{C_{P1}} \int I_{in}(t)dt = \frac{q_{in}}{C_{P1}} \tag{3}$$

$$\begin{aligned} V_G &= \frac{1}{C_{P2} r_{x2}} \int V_1(t)dt \\ &= \frac{1}{C_{P2} \, r_{x2}} \int \frac{q_{in}(t)}{C_{P1}} dt \\ &= \frac{g_{m2}}{C_{P1} C_{P2}} \int q_{in}(t)dt \end{aligned} \tag{4}$$

where μ_n, C_{ox} are respectively the electron mobility and gate capacitor, while W/L is the transistor dimensions. The fact that this resistance can be controlled via the biasing current I_B is very beneficial from IC integration point of view.

The required multiplication operation is realized by the current-voltage relationship of the NMOS transistor arranged to operate in the triode region:

$$I_Z = \underbrace{\mu_n C_{OX} \left(\frac{W}{L} \right)}_{\beta} (V_{GS} - V_{TN}) V_{DS}, \quad I_Z = \frac{V_1}{r_{x3}} \tag{5}$$

By using (3) and (4) in (5), the equation is obtained as follows:

$$\frac{q_{in}}{r_{x3} C_{P1}} = \beta \left(\frac{g_{m2}}{C_{P1} C_{P2}} \int q_{in}(t)dt - V_{TN} \right) V_{in} \tag{6}$$

The Eq.6 is rearranged as follows:

$$C_M = \frac{q_{in}}{V_{in}} = \frac{\beta C_{P1}}{g_{m3}} \left(\frac{g_{m2}}{C_{P1} C_{P2}} \int q_{in}(t)dt - V_{TN} \right) \tag{7}$$

By considering the charge-voltage relation of the capacitor element $q(t) = C\,v(t)$, and rearranging the equation, the value of memcapacitor becomes as follows:

$$C_M = \frac{\beta C_{P1}}{g_{m3}} \left(\frac{g_{m2}}{C_{P1} C_{P2}} \int q_{in}(t)dt - V_{TN} \right) \tag{8}$$

$$C_M = \frac{\beta g_{m2}}{g_{m3} C_{P2}} \int q_{in}(t)dt - \frac{\beta_1 C_{P1}}{g_{m3}} V_{TN} \tag{9}$$

From Eq. 9, the value of the memcapacitance consists of two terms, one being time-dependent and the other is constant. Both of the terms can be electronically adjusted by changing g_{m2} and g_{m3} parameters, which may be beneficial in practical applications of the memcapacitance.

In Table I, aspect ratios of the MOS transistors used in active devices are given.

TABLE I
ASPECT RATIOS (in μm) OF THE TRANSISTORS IN FIG.2

MOS transistor	CCCII and CCII
M1, M2	4/0.8
M3, M4	10/0.8
M5	2/0.8
M6	5/0.8
M7	1.5/0.8
M8	4/0.8
M_B	35/0.8

The CCCII active element is depicted in Fig.2a and realized by using conventional translinear topology. To implement the CCII, input transistor with a very low r_x value is selected in accordance with Eq. 1. Voltage buffer is also shown in Fig.2b.
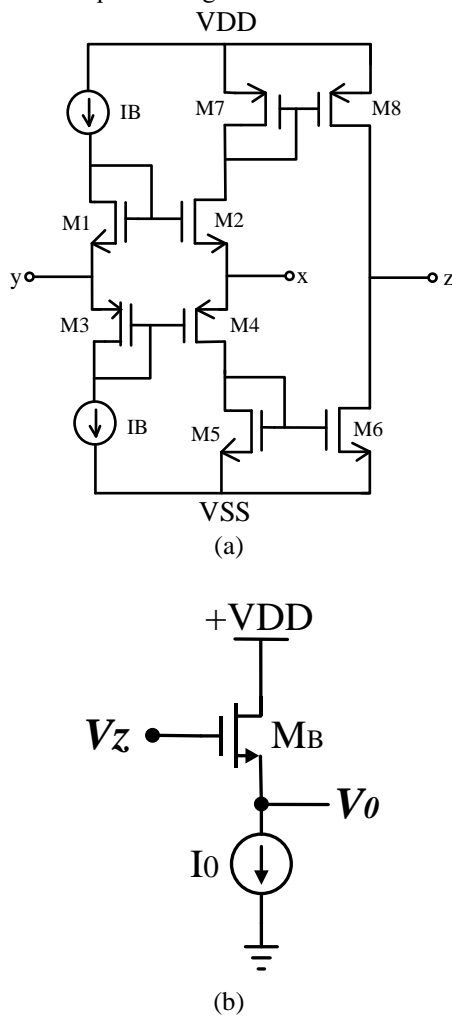

(a)

(b)

Fig.2. Implementations of (a) the current conveyors,
(b) the voltage buffer

III. NON-IDEAL ANALYSIS OF THE MEMCAPACITOR EMULATOR

Non-ideal model of the proposed memcapacitor is shown in Fig.3. Considering the well-known non-idealities of the active elements, memcapacitor defining equation is obtained as follows [24]:

$$V_1 = [\alpha_1(s)\beta_1(s)\gamma_1(s)\frac{1}{\left(\frac{1}{r_{z1}} + sC_{P1}\right)}]I_{in} \qquad (10)$$

In this expression, $\alpha_1(s)$ and $\beta_1(s)$ are respectively, the non-ideal current and voltage gains of CCII, $\gamma_1(s)$ is the non-ideal gain of the buffer, while r_{z1} is the z-terminal parasitic resistance.

Extensive simulation results of the circuit in Fig. 2a shows that frequency dependency of $\beta_1(s)$ and $\gamma_1(s)$ can be neglected, while $\alpha_1(s)$ can be represented with the following simple expression:

$$\alpha_1(s) = \alpha_0 \frac{\omega_z}{s + \omega_z} \qquad (11)$$

For practical applications, the output resistance of the CCII satisfy the following: $(1/r_{z1} \ll |j\omega C_{P1}|)$, thus Eq.10 can be approximated as:

$$V_1 \cong = \frac{\alpha_1(s)}{C_{P1}} \frac{I_{in}}{s} = \frac{\alpha_1(s)}{C_{P1}} q_{in} \qquad (12)$$

Considering the non-idealities of integrator-2, the equations are obtained as follows:

$$V_G = [\alpha_2(s)\beta_2(s)\gamma_2(s)g_{m2} \frac{1}{\left(sC_{P2} + \frac{1}{r_{z2}}\right)}]V_1 \qquad (13)$$

Assuming that $(1/r_{z2} \ll |j\omega C_{P2}|)$ and $\beta_2(s)$ and $\gamma_2(s)$ are constant, Eq.13 can be obtained as:

$$V_G \cong \left[\alpha_2(s)g_{m2} \frac{1}{C_{P2}}\right]\frac{V_1}{s} \qquad (14)$$

Using (12) into (14) yields:

$$V_G = \left[\alpha_1(s)\alpha_2(s)g_{m2} \frac{1}{C_{P1}C_{P2}}\right]\frac{q_{in}}{s} \qquad (15)$$

If the current-voltage relation of the NMOS transistor operating in the linear region is written and the Eq.15 is substituted in this relation, the memcapacitance relation is obtained as follows:

$$I_Z - \frac{V_{in}}{r_{z3}} = \beta(V_{GS} - V_{TN})V_{DS}, \quad I_Z = \frac{V_1}{r_{x3}} \qquad (16)$$

$$\frac{V_1}{r_{x3}} - [\frac{V_{in}}{r_{z3}} + \frac{V_{in}}{r_{Y1}} + V_{in}(sC_{Y1})]$$
$$= \beta[(\alpha_1(s)\alpha_2(s)g_{m2} \frac{1}{C_{P1}C_{P2}})\frac{q_{in}}{s} \qquad (17)$$
$$- V_{TN}]V_{in}$$

Rearranging this equation, memcapacitance value can be obtained as:

$$\frac{\alpha(s)}{C_{P1}r_{x3}}q_{in} = \left[\beta\alpha^2(s)g_{m2}\frac{1}{C_{P1}C_{P2}}\frac{q_{in}}{s} - \beta V_{TN} + \frac{1}{r_{z3}}\right.$$
$$\left. + sC_{Y1}\right]V_{in},$$
$$\alpha_1(s) = \alpha_2(s) = \alpha(s) \tag{18}$$

$$C_M = \frac{q_{in}}{V_{in}} = \underbrace{\frac{\beta\alpha(s)g_{m2}}{g_{m3}C_{P2}}\int q_{in}(t)dt - \frac{\beta C_{P1}}{\alpha(s)g_{m3}}V_{TN}}_{Ideal\ memcapacitor}$$
$$+ \frac{C_{P1}}{\alpha(s)g_{m3}}\left(\frac{1}{r_{z3}} + \frac{1}{r_{Y1}} + sC_{Y1}\right) \tag{19}$$

As it can be seen from Eq.19, in the non-ideal case, the parasitics C_{Y1}, r_{Y1} and r_{z3} appear in parallel with the memcapacitor. In case, the circuit driving this memcapacitor has a lower output impedance, these effects can be neglected. Furthermore, the frequency dependency of the current gain, $\alpha(s)$ may worsen the memory behavior of the element. Therefore, the circuit operating frequency range should be kept much smaller than the pole in the model of Eq. (19).
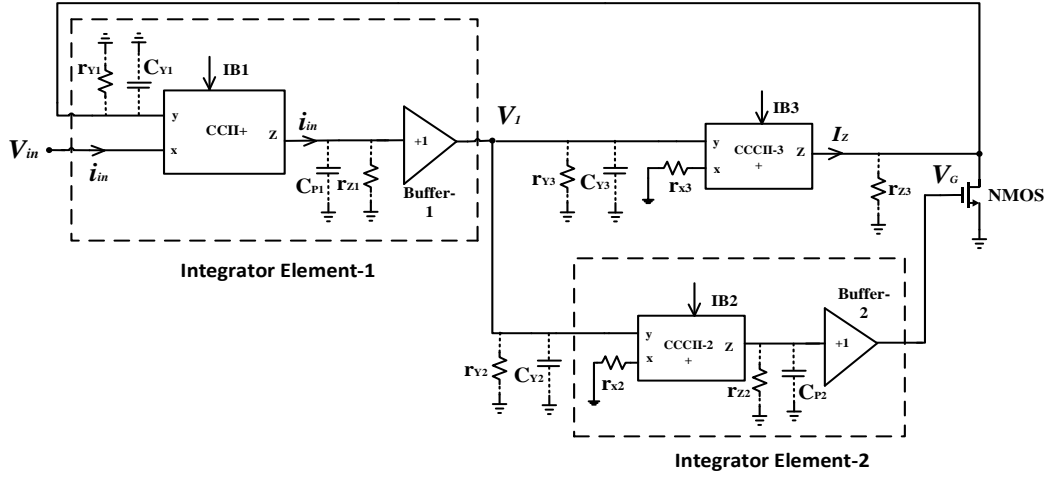

Fig.3. Non-ideal model of proposed memcapacitor

IV. SIMULATION RESULTS

The simulation results of the proposed circuit are produced by using UMC 0.18 μm technology parameters in Cadence design environment. The active elements, CCII, CCCII and voltage buffers are supplied with ± 1V. Since the input current on the parasitic capacitor cannot be sensed, the hysteresis loop is simulated depending on the input voltage (V_{in}) and $V_1(q_{in}/C_{p1})$ which is the first integrator output.
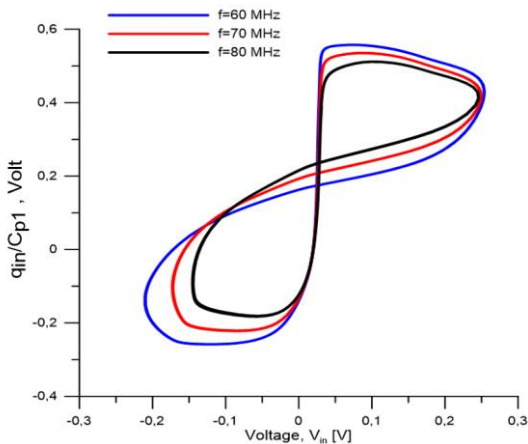
An external sinusoidal signal with an amplitude of 200 mV is applied to the circuit to obtain the emulator characteristic. As shown in Fig. 4, the circuit generates the pinched hysteresis characteristic which is the fingerprint of mem-behavior. The sample characteristics are given at three different frequencies, at 60 MHz, 70 MHz and 80 MHz.

However, the simulation results for different biasing currents are also obtained in Fig.5. From these results, it is seen that the circuit is capable of generating the memristor behavior over a wide range of the biasing current

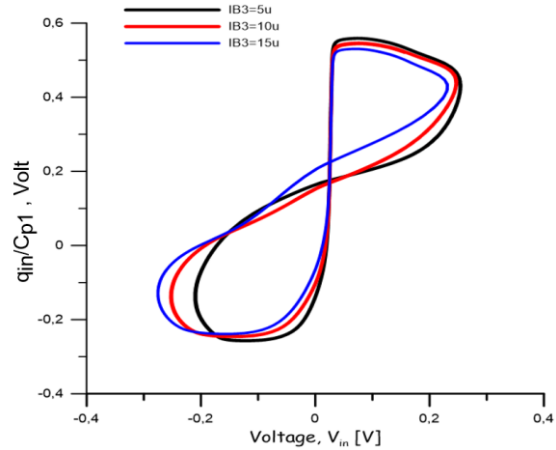Fig.4. The Voltage–charge characteristic of proposed memcapacitor.

Fig.5. Pinched hysteresis loops for different biasing currents

The change in the circuit performance against environmental temperature variations is also studied. The circuit dynamics at three different temperatures are obtained at 60 MHz and the results are given in Fig. 6. From these results, it is clear that the circuit is able to generate the mem-behavior over a wide range of temperature. In addition, simulation results at different processing corners are obtained at 60 MHz and are given in Fig.7. From these results, the circuit works properly against the process changes.
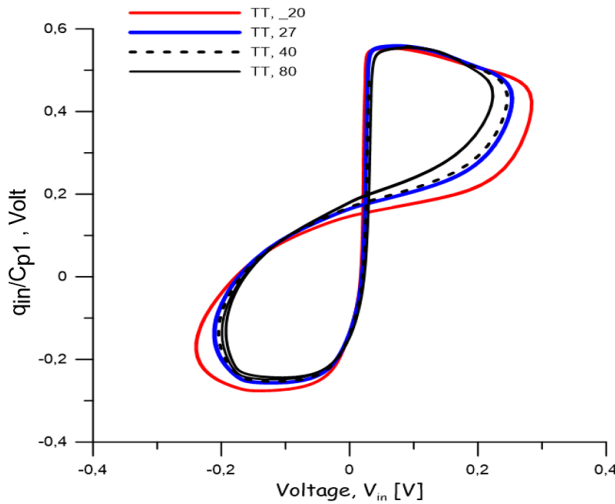

Fig.6. Memcapacitive characteristics at three different temperatures
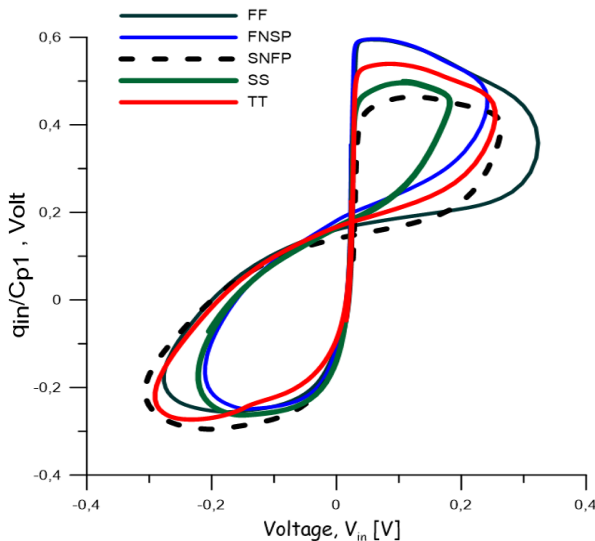

Fig.7. Memcapacitive characteristics for the process corners

In order to reveal the dependency of the memcapacitance to the variation of the input signal, we have obtained the simulation result in Fig.8. The memcapacitance depends on the input signal frequency, which is resulted from the nonlinearity of the memcapacitor.

Since intrinsic capacity is used instead of discrete capacity in this study, the capacity value varies between 100-500 fF. The rate of change is in the same order as circuits using discrete capacity [14].
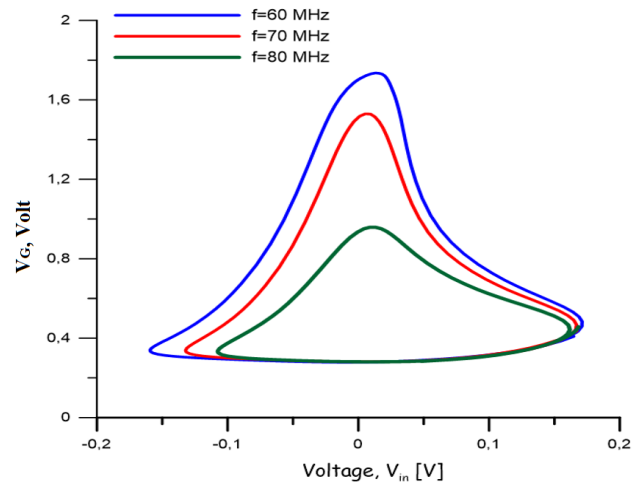

Fig.8. V_G versus V_{in} for different operating frequencies

V. MC MODIFIED FOR WIDE OPERATING FREQUENCY RANGE

The proposed memcapacitor has an operating frequency range proportional to g_m/C_P. As we use an intrinsic capacitor with a small range of values to implement C_p, the operating frequency range of the circuit varies within a narrow range. To remedy this issue, capacitance multiplier is proposed in the literature [25]. In this section, we applied this technique to the proposed emulator, in order to expand its operation frequency range, towards lower frequency region.

A conceptual capacitance multiplier built around CCII- is given in Fig.9. CCII- refers to the negative output current conveyor and the constitutive equation is given as:

$$i_y = 0, \qquad V_x = V_y, \qquad i_z = -K_C i_x \tag{20}$$

where KC is the current gain from the x to z terminal currents of the current conveyors and equals 1 for conventional current conveyors. The current gain mentioned in this study should be taken as greater than 1. In this case, the equivalent input capacitance can be calculated using the following equation:
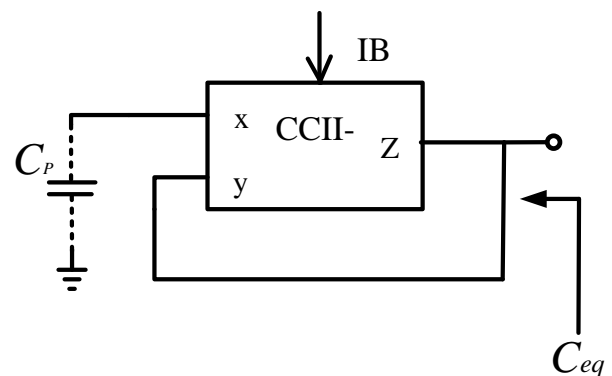
$$C_{eq} = K_C C_P \tag{21}$$

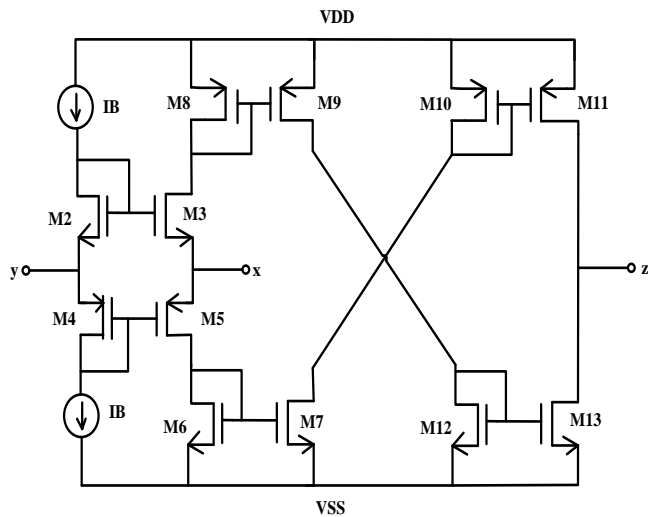Fig.9. Capacitance multiplier built around a CCII [25]

Fig.10. CMOS realization of the CCII- [26]

Therefore, for $K_C > 1$, the equivalent capacity will be greater than the C_p capacity. The Kc value can be set to the desired value by appropriately arranging the size ratios of the M10-M11 and M12-M13 MOS current mirrors transistors in the translinear current conveyor which is shown in Figure 10.

By applying this technique to the proposed circuit, we obtain the modified circuit in Fig. 11. Assuming that the input terminal voltages of the current conveyors are equal, the memcapacitance of the circuit in Fig. 11 is as follows:

$$C_M = \frac{\beta g_{m2}}{g_{m3} K_C C_{P2}} \int q_{in}(t)dt \ - \frac{\beta_1 C_{P1}}{g_{m3}} V_{TN} \qquad (22)$$

To verify the feasibility of the approach, simulation results are obtained for the 80 MHz and 100 mV input sinusoid of the modified circuit. The observed pinched hysteresis loops obtained for $K_C =10$ and $K_C =1$ are shown in Fig.12.
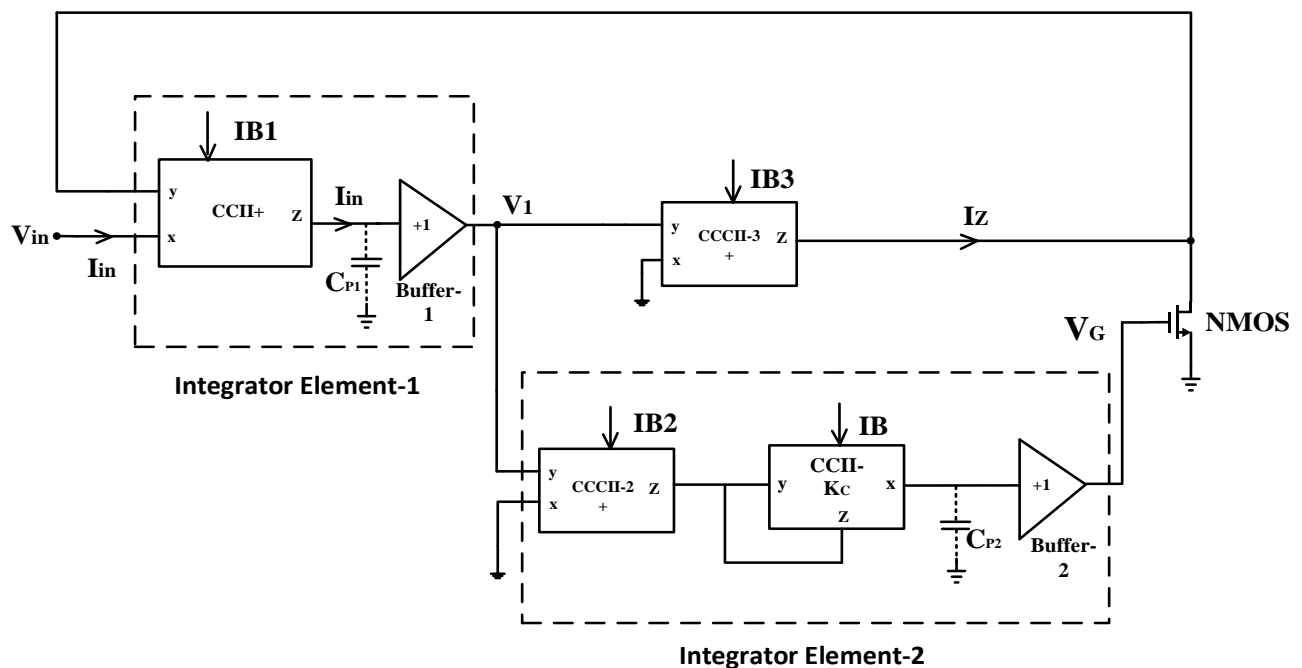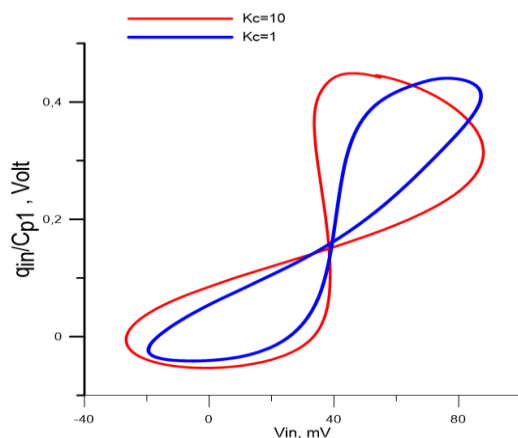

Fig.11. The memcapacitor emulator modified for low operating frequency

Fig.12. Voltage–current response of the modified MC
for $K_C =1$ and $K_C =10$

VI. COMPARISON OF THE PROPOSED MC WITH EXISTING CIRCUITS

Some figures which can be useful to compare the proposed circuit compared with its existing counterparts are presented in Table II. All existing counterpart's studies are used passive components, so they are not area efficient design. To the best of the authors knowledge, there is not any other active-only memcapacitor emulator in the literature. It provides a big advantage in terms of the IC design environment, as it takes up less space as there are no discrete components.

TABLE II
PERFORMANCE COMPARISON WITH OTHER STUDIES

References	Number of active components	Operating frequency	Power supply	Number of passive elements	Elec. Tunability	Floating & grounded	Transistor Parameter
[12]	1 CBTA, 1 Memristor	250kHz	NA	1C	Yes	Floating	TSMC 0.18 µm
[13]	5 Opamp, 1 Multiplier	200Hz	±15V	11R, 2C 1Diode	No	Grounded	Discrete components
[14]	2 CCII, 1 Multiplier	48Hz	±20V	3C, 2R	Yes	Grounded	Discrete components
[15]	1 DVCCTA	900kHz	±0.9V	2C, 1R	No	Grounded	TSMC 0.18µm
[16]	2 OTA, 1 multiplier	10Hz	±1.25V	2C, 2R	Yes	Grounded	TSMC 0.18µm
[17]	1 DXCCDITA	1MHz	±1.25V	2R, 1C	Yes	Floating	CMOS technology 0.18µm
[18]	3 Opamp, 2 CFOA	10Hz	NA	3R, 2C, 1LDR	No	Grounded	Discrete components
[19]	2 AD844, 1 Memristor	10Hz	NA	1C, 1R	No	Grounded	NA (simulation)
[20]	1 Multiplier, 4 Opamps, 1CCCS	10Hz	±10V	3C, 2R	No	Grounded	NA (simulation)
Proposed work	2 CCCII, 1CCII and 2 buffers	80MHz	±1V	**No passive component**	Yes	Grounded	**UMC 0.18 µm**

As can be seen from Table II, the proposed circuit can operate at much higher frequencies and lower power supply rates than existing circuits. The proposed memcapacitor can be adjusted electronically in this study, as in some studies in Table II. The floating solution offers more flexible usage possibilities, but the grounded solutions are used more in practice because they have a simpler structure.

VII. CONCLUSION

In this study, an integrator-based memcapacitor emulator is presented. The important parameters of the proposed circuit can be adjusted electronically to the desired value. Compared to previous studies presented in the literature, the proposed memcapacitor has a structure consisting of only active building blocks. Therefore, the chip area will be smaller compared to their counterparts. The viability of the circuit is verified via detailed simulation results. Furthermore, a detailed nonideality analysis which reveals the main limitation of the circuit are presented. Finally, a modification technique which can be applied to extend the operating frequency range of the circuit is presented.

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BIOGRAPHIES

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